Remarks

The Final Office Action dated January 15, 2008, lists the following rejection: claims 1-5 and 7-18 stand rejected under 35 U.S.C. § 102(b) over Omura *et al.* (U.S. Patent Pub. 2002/0030237). Claims 9-10 are objected to as being dependent upon a rejected base claim but would be allowable if rewritten in independent form.

Applicant respectfully traverses the § 102(b) rejection of claims 1-5 and 7-18 because the cited portions of the Omura reference do not correspond to the claimed invention which includes, for example, aspects directed to first and second capacitive voltage coupling regions that are provided to apply the same voltages to the field shaping region as are applied to the pn junction. The Examiner erroneously asserts that Omura's buried electrode 17 and gate electrode 19 correspond to the claimed first and second capacitive voltage coupling regions respectively. Omura does not teach that buried electrode 17 and gate electrode 19 are provided to apply the same voltages to first insulating film 16 as are applied to the junction between well layer 13 and drift layer 12. *See, e.g.,* Figure 4.

More specifically, Omura teaches that drain electrode 20 serves as the first main electrode and that source electrode 21 serves as the second main electrode, which apply a voltage to the junction between well layer 13 and drift layer 12. *See, e.g.,* Paragraph 0059. Omura's buried electrode 17 may be connected to source electrode 21 or to drain electrode 20; however, Omura's gate electrode 19 is not connected to either source electrode 21 or to drain electrode 20 (*e.g.,* gate electrode 19 is insulated from source electrode 21). *See, e.g.,* Paragraphs 0060 and 0062. Thus, Omura's buried electrode 17 and gate electrode 19 are not provided to apply the same voltages to insulating film 16 as are applied to the junction between well layer 13 and drift layer 12 by source electrode 21 and drain electrode 20. Therefore, Omura's buried electrode 17 and gate electrode 19 do not correspond to the claimed first and second capacitive voltage coupling regions. Accordingly, the § 102(b) rejection of claims 1-5 and 7-18 is improper and Applicant requests that it be withdrawn.

Applicant further traverses the § 102(b) rejection of claims 2-4 because the Examiner appears to take Official Notice of facts without citing a prior art reference in support of this conclusion. According to M.P.E.P. § 2144.03, "It would not be

appropriate for the examiner to take official notice of facts without citing a prior art reference where the facts asserted to be well known are not capable of instant and unquestionable demonstration as being well-known." Applicant notes that Official Notice without documentary evidence to support an Examiner's conclusion is permissible only in some circumstances and that these circumstances should be rare when an application is under final rejection. *See, e.g.,* M.P.E.P. § 2144.03.

In this instance, the Examiner acknowledges that the Omura reference does not disclose the use of the claimed materials for the field shaping region. The Examiner then asserts that it would be obvious to use the claimed materials for Omura's insulating film 16. However, the Examiner has not cited any reference in support of the conclusion that use of the claimed materials is well known and the Examiner has also not provided any reason why the skilled artisan would use the claimed materials for the insulating film 16 in the Omura reference. This approach is contrary to the requirements of § 103 and relevant law. *See, e.g., KSR Int'l Co. v. Teleflex Inc.*, 127 S. Ct. 1727, 1741 (U.S. 2007)

> Although common sense directs one to look with care at a patent application that claims as innovation the combination of two known devices according to their established functions, it can be important to identify a reason that would have prompted a person of ordinary skill in the relevant field to combine the elements in the way the claimed new invention does. This is so because inventions in most, if not all, instances rely upon building blocks long since uncovered, and claimed discoveries almost of necessity will be combinations of what, in some sense, is already known.

Moreover, Applicant submits that Omura appears to teach away from using a material with a high dielectric constant for insulating film 16. For example, Omura teaches that using a material having a dielectric constant about 1/3 that of silicon for insulating film 16 results in an increase in the breakdown voltage. *See, e.g.,* Paragraph 0085. In contrast, tantalum oxide Ta_2O_5 (*see, e.g.,* claim 4) has a dielectric constant that is almost twice that of silicon. *See, e.g.,* Paragraph 0028, lines 15-20 of Applicant's specification.

In view of the above, the § 102(b) rejection of claims 2-4 is improper and Applicant requests that it be withdrawn. Should any rejection of claims 2-4 based upon the Omura reference be maintained, Applicant requests that the Examiner provide support for the conclusion that the use of the claimed materials is well known and that the

Examiner provide a reason why the skilled artisan would modify Omura to use the claimed materials.

Applicant further traverses the § 102(b) rejection of claim 13 because the cited portions of Omura do not correspond to aspects of the claimed invention directed to the field shaping region being separated from the semiconductor region having the pn junction by an insulating region. Omura does not teach that there is an insulating region that separates insulating film 16 from drift layer 12. As is shown by Omura in Figure 4, there is not an insulating region between insulating film 16 and drift layer 12. Accordingly, the § 102(b) rejection of claim 13 is improper and Applicant requests that it be withdrawn.

Applicant further traverses the § 102(b) rejection of claims 14-18 because these claims recite structural features that have been improperly ignored by the Examiner. For example, claim 14 recites that the device is a diode and the pn junction is the rectifying junction of the diode. In another example, claim 16 recites that the device is a field effect transistor. These claims state what the device is (*i.e.,* structure), not how the device is used (*i.e.,* function). For instance, one of skill in the art would recognize the structure of a diode and a FET without using the diode or the FET. Accordingly, these limitations cannot be properly construed as having only functional characteristics as the use of the corresponding structure is not necessary to identify the structure. Therefore, the § 102(b) rejection of claims 14-18 is improper and Applicant requests that it be withdrawn.

In view of the remarks above, Applicant believes that each of the rejections has been overcome and the application is in condition for allowance. Should there be any remaining issues that could be readily addressed over the telephone, the Examiner is asked to contact the agent overseeing the application file, Peter Zawilski, of NXP Corporation at (408) 474-9063 (or the undersigned).

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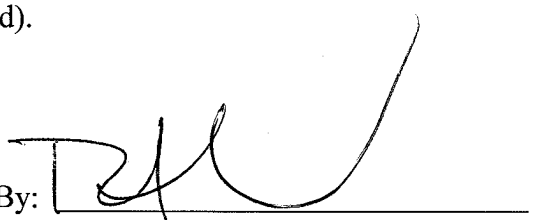
By: 
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